REMARKS

Summary of Office Action

Claims 1-39 were pending in the above-identified patent application.

The abstract of the disclosure was objected to for failing to list "ABSTRACT" as the heading.

Claims 1-13, 15, and 18-39 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kenney et al. U.S. Patent No. 6,803,827 (hereinafter "Kenney"). Claims 14, 16, and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kenney in view of Brunn et. al. U.S. Patent No. 6,650,195 (hereinafter "Brunn").

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Summary of Applicants' Reply

Applicants have amended the abstract to overcome the objection.

Applicants have amended claims 18, 19, 29, and 30 to more particularly define the claimed invention. Applicants have also cancelled claims 20 and 31 without prejudice. The claim amendments are fully supported by the originally filed specification and do not introduce new matter (see, e.g., applicants' specification at FIG. 2B; pp. 19 and 20, ¶¶ 47 and 48; and originally-filed claims 20 and 31).

The Examiner's objection and rejections are respectfully traversed.

Summary of Telephonic Interview

Applicants would like to thank Examiners Browne and Brown for the courtesies extended during the February 16, 2006 telephonic interview with the undersigned and Mr. Gall Gotfried. During the interview, the Examiner's rejections with respect to independent claims 1, 18, and 29 in view of Kenney were discussed.

With respect to claim 1, applicants contended that Kenney does not show applicants' claimed feature of a divider circuit whose output feeds back to the input of a phase frequency detector. Instead, applicants contended that Kenney describes a separate phase detector and a frequency detector circuit where the output of a divider circuit is sent as input to the frequency detector circuit. Examiner Browne conceded that Kenney does not show all the features of applicants' claim 1 and indicated that a further search would be required.

Applicants proposed amending independent claims 18 and 29 to more particularly specify that the control circuitry is capable of adjusting the bandwidth in different components of the CDR and PLL circuitry. Applicants contended that Kenney only describes adjusting the frequency in a tunable oscillator. Examiner Browne indicated that this proposed amendment appeared to overcome Kenney but would require a further search.

Applicants' Reply to the
Objection to the Abstract

The abstract of the disclosure was objected to for failing to list "ABSTRACT" as the heading.

Applicants have amended the abstract of the disclosure to include a heading entitled "Abstract." Accordingly, applicants respectfully request that the objection be withdrawn.

Applicants' Reply to the
Rejection of the Claims

Claims 1-13, 15, 18, 19, 21-30, and 32-39 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kenney. Claims 14, 16, and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kenney in view of Brunn.

Claims 1-17

Applicants' independent claim 1 is directed to circuitry for providing a dynamically adjustable bandwidth. The circuitry includes a phase frequency detector whose output is coupled to a charge pump. The circuitry also includes a divider circuit whose output feeds back to the input of the phase frequency detector. The circuitry further includes control circuitry that receives a control signal used to dynamically adjust a setting in at least one of the charge pump, a loop filter, a voltage controlled oscillator, and the divider circuitry.

The Examiner cited to FIGS. 2-4 of Kenney as allegedly showing all the features of applicants' independent claim 1. In particular, the Examiner contended that (1) applicants' phase frequency detector is phase detector 108a in FIG. 3 of Kenney and (2) applicants' divider circuit is frequency divider circuit 162 in FIG. 3 of Kenney. Office Action, pp. 2-3.

Applicants respectfully submit that Kenney does not show or suggest all the features of applicants' independent

claim 1. More particularly, Kenney does not show or suggest applicants' claimed feature of a divider circuit whose output feeds back to the input of the phase frequency detector. Instead, FIG. 3 and the corresponding description of Kenney describe a separate phase detector 108a and frequency detector system 126a. The output of phase detector 108a is coupled to charge pump 150. The output of frequency divider circuit 162 is coupled to frequency detector system 126, and does not feed back to phase detector 108a. Kenney at FIG. 3; col. 6, l. 60 to col. 7, l. 40.

For at least the foregoing reasons, applicants respectfully submit that independent claim 1 is allowable over Kenney. Claims 2-17, which depend from claim 1, are therefore also allowable over Kenney.

Claims 18, 19, 21-30, and 32-39

Applicants' independent claims 18 and 29, as amended, are directed to a programmable logic device having a clock data recovery (CDR) circuitry (claim 18) or phase locked loop (PLL) circuitry (claim 29), and control circuitry. The CDR/PLL circuitry uses a clock signal to produce a recovered clock signal having a phase and frequency which correspond to the phase and frequency of the clock signal. Control circuitry receives a control signal and dynamically adjusts the bandwidth of the CDR/PLL circuitry by changing a setting in at least one component in the CDR/PLL circuitry. The control circuitry is capable of changing the setting in a charge pump, a loop filter, a voltage controlled oscillator, and a divider circuit in the CDR/PLL circuitry.

Applicants respectfully submit that Kenney does not show or suggest applicants' claimed feature of a programmable logic device having control circuitry that is capable of changing the setting (to dynamically adjust the bandwidth) of a charge pump, a loop filter, a voltage controlled oscillator, and a divider circuit in CDR/PLL circuitry.

Broadly speaking, Kenney describes a frequency acquisition system for a tunable oscillator that uses a phase locked loop (PLL) and/or a frequency locked loop (FLL). As shown and described in connection with FIGS. 2-4 of Kenney, the frequency of voltage controlled oscillator (VCO) 112 can be adjusted by making fine adjustments to the voltage of VCO 112 in the PLL circuitry or by making coarse adjustments to the voltage of VCO 112 in the FLL circuitry. See, e.g., Kenney at FIGS. 2-4; col. 5, l. 40 to col. 8, l. 23.

Kenney describes a frequency acquisition system that can only adjust the frequency of a tunable oscillator. Kenney does not show or suggest that the system is further capable of dynamically adjusting its other components (i.e., charge pump, loop filter, divider circuit) as recited in applicants' independent claims 18 and 29.

For at least the foregoing reasons, applicants respectfully submit that independent claims 18 and 29 are allowable over Kenney. Dependent claims 19, 21-30, and 32-39, which depend from respective independent claims 18 and 29, are therefore also allowable over Kenney.

Conclusion

Applicants respectfully submit that this application is in condition for allowance. Accordingly, prompt

consideration and allowance of this application are respectfully requested.

Respectfully submitted,

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